

**Department of Electrical Engineering**

**Optional 4: MOD-10**

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Class: EE 301

Date Due: December 11, 2017

**Explanation**

For this lab, the goal is to change the asynchronous up counter from lab 5 into a modulus counter, which count up to ten states from zero to nine before returning back to the zero state. For this to happen, the design must ensure that when the output reaches nine (‘1001’), a signal is sent to the clear input to reset everything back to the original state. To accomplish this, when the output reaches ‘1010’, the high outputs of the first and third flip flop will be combined into a NAND gate with the output connected to the clear input to allow for the output to return to zero. With this change, a waveform was generated and the design was tested on the board.

**Code for JK flip flop**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity jkff is

Port ( j : in STD\_LOGIC;

k : in STD\_LOGIC;

clr : in STD\_LOGIC;

clk : in STD\_LOGIC;

q,qn: out STD\_LOGIC);

end jkff\_2;

architecture Behavioral of jkff is

signal s : std\_logic := '0';

begin

Process (clk,j,k,s,clr)

begin

if (clk' EVENT and clk = '1') then

if clr = '0' then s <= '0';

else

if j = '0' and k = '0' then s <= s;

elsif j = '0' and k = '1' then s <= '0';

elsif j = '1' and k = '0' then s <= '1';

Else s <= not s;

end if;

end if;

end if;

q <= s;

qn <= not s;

end process;

end Behavioral;

**Structural Code**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity Mod10 is

Port ( clock : in STD\_LOGIC;

Q : out STD\_LOGIC\_VECTOR (3 downto 0));

end Mod10;

architecture Behavioral of Mod10 is

component jkff

Port ( j : in STD\_LOGIC;

k : in STD\_LOGIC;

clr : in STD\_LOGIC;

clk : in STD\_LOGIC;

q,qn: out STD\_LOGIC);

end component;

signal s : std\_logic\_vector(3 downto 0) := "0000";

signal clr,a,b,c,d: std\_logic ;

begin

clr <= (s(1) nand s(3));

R1: jkff port map('1','1',clock,clr,s(0),a);

R2: jkff port map('1','1',s(0),clr,s(1),b);

R3: jkff port map('1','1',s(1),clr,s(2),c);

R4: jkff port map('1','1',s(2),clr,s(3),d);

Q <= s;

end Behavioral;

**TESTBENCH**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

ENTITY Mod10\_Test IS

END Mod10\_Test;

ARCHITECTURE behavior OF Mod10\_Test IS

COMPONENT Mod10

Port ( clock : in STD\_LOGIC;

Q : out STD\_LOGIC\_VECTOR (3 downto 0));

END COMPONENT;

signal clock : std\_logic := '0';

signal Q : std\_logic\_vector(3 downto 0);

constant clock\_period : time := 10 ns;

BEGIN

uut: Mod10 PORT MAP (

clock => clock,

Q => Q );

clock\_process :process

begin

clock <= '0';

wait for clock\_period/2;

clock <= '1';

wait for clock\_period/2;

end process;

stim\_proc: process

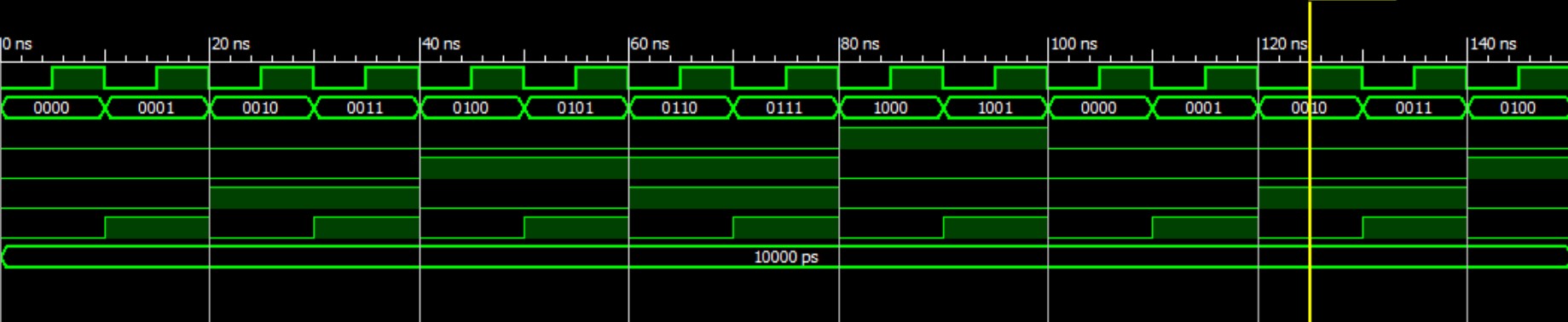
begin

wait;

end process;

END;

**WaveForm**



**Constraint File**

NET "clock" CLOCK\_DEDICATED\_ROUTE = FALSE;

NET "clock" LOC = "G12";

NET "Q(0)" LOC = "M5" ;

NET "Q(1)" LOC = "M11" ;

NET "Q(2)" LOC = "P7" ;

NET "Q(3)" LOC = "P6" ;